CIRCUIT AND SYSTEM FOR ADDRESSING MEMORY MODULES

## ABSTRACT OF THE DISCLOSURE

A circuit and system addressing multiple computer memory modules on the same bus while maintaining proper timing. The circuit includes a transmission line having a dampening impedance between a driver and a branch point of the transmission line. The circuit also has a termination impedance having one end coupled to the transmission line between the dampening impedance and the branch point. The transmission line has branches from the branch point. Individual branches are coupled to at least one memory module interface.